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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/846,681	05/01/2001	Jeffrey Robert Perry	50019.44US01/P04884	2920

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EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/846,681	PERRY ET AL.	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *June 27, 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to patent application S/N: 09/846,681, filed on 05/01/01. Claims 1-25 are pending in this Action.

Drawings

The drawings filed on 06/27/2003 are acceptable for examination.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown, Don, US patent application publication no. US 2002/0156757 in view of Valainis et al, US patent no. 6,389,582 B1.

As per claim 1, Brown discloses a method and system for analyzing, designing and making integrated circuit product over a computer network with feature limitations very similar to the claimed invention (Field of the Invention and Summary of the Patent). According to Brown, the design analysis and simulation method includes:

Identifying circuit component under design to be thermally simulated over the network (page 5, paragraphs [0054], [0055]) for example,

Determining thermal characteristics for a set of circuit components in design [0063] to [0065] for thermal simulation,

Performing thermal simulation for the design ([0055] [0076], [0083], [0087], for example),

Producing result based on thermal design and simulation process in tool (28) as above, and providing the result to the user over a network as claimed. Brown does not expressly disclose the thermal analysis for final component placement on board layout as cited in the preamble. Such feature is however well known in the art. In fact, Valainis teaches a method and system for analyzing thermal generation in the final circuit placement on design board (see Summary of the Invention). Such thermal analysis provides an effective to place components into the design, change the design physical process, component changes, placement changes, etc. (col. 3, lines 9-24, col. 5, lines 1-12, col. 6, lines 42-64).

This would motivate practitioner in the art at the time of the invention was made to combine the teaching in Valainis into the Brown thermal simulator in order to simulate component placement into the integrated circuit design board in a final phase of the design process to make any placement change, optimize placement design process change, etc to meet design and thermal performance of the circuit.

As per claim 2, Brown and Valainis disclose circuit characteristics being used in the thermal analysis, design characteristics changes for the simulation, etc. as claimed.

As per claim 3, Brown discloses the simulation process is performed over the computer network (pages 5-7).

As per claim 4, Brown discloses documentations for the design process and simulation of the products.

As per claims 5-6, Brown discloses the simulator system allows user to share simulation resources, simulation data, design data, etc. Brown also discloses output devices being used to plot and print out simulation results [0078]-[0094] as claimed.

As per claims 7-9, Brown and Valainis disclose display of temperature intensity of the across the boar, graphical layout of the design, thermal characteristics, heat sink in vendor supply, etc. as claimed.

As per claims 10-12, Brown discloses the circuit design at the board level, which would include adding fan and airflow for ventilation in the design to minimize heat radiation.

As per claim 13, Brown discloses a method and system for analyzing, designing and making integrated circuit product over a computer network with feature limitations very similar to the claimed invention (Field of the Invention and Summary of the Patent). According to Brown, the design simulation method includes:

Identifying circuit component under design to be thermally simulated over the network (page 5, paragraphs [0054], [0055]) for example,

Determining thermal characteristics for a set of circuit components in design [0063] to [0065] for thermal simulation,

Performing thermal simulation for the design ([0055] [0076], [0083], [0087], for example),

Producing result based on thermal design and simulation tool (28) as above, and providing the result to the user over a network as claimed. Brown does not expressly disclose the thermal analysis for final component placement on board layout as cited in the preamble. Such feature is however well known in the art. In fact, Valainis teaches a method and system for analyzing thermal generation in the circuit final placement on design board (see Summary of the Invention). Such thermal analysis provides an effective to place components into the design, change the design physical process, component changes, etc. (col. 3, lines 9-24, col. 5, lines 1-12, col. 6, lines 42-64).

This would motivate practitioner in the art at the time of the invention was made to combine the teaching in Valainis into the Brown thermal simulator in order to simulate component placement into the integrated circuit design board in a final phase of the design process to make placement change, optimize placement process changes, etc to meet thermal performance of the design circuit.

As per claim 14, Brown and Valainis disclose circuit characteristics being used in the thermal analysis, design characteristics changes for the simulation, etc. as claimed.

As per claim 15, Brown discloses the simulation process is performed over the computer network (pages 5-7).

As per claim 16, Brown discloses documentations for the design process and simulation of the products.

As per claims 17 and 18, Brown discloses the simulator system allows user to share simulation resources, simulation data, design data, etc. Brown also discloses output devices being used to plot and print out simulation results, graphical layout of the circuit and the final design product [0078]-[0094] and [0114] to [0120] as claimed.

As per claim 19, Brown discloses a method and system for analyzing, designing and making integrated circuit product over a computer network with feature limitations very similar to the claimed invention (Field of the Invention and Summary of the Patent). According to Brown, the design simulation system includes

A client connected to a simulation network to simulate a thermal system,

A server having a server network connection device operative to connect the server to the network (Figs. 1-3), and means for

Identifying circuit component under design to be thermally simulated over the network (page 5, paragraphs [0054], [0055]) for example,

Determining thermal characteristics for a set of circuit components in design [0063] to [0065] for thermal simulation,

Performing thermal simulation for the design ([0055] [0076], [0083], [0087], for example),

Producing result based on thermal design and simulation tool (28) as above, and providing the result to the user over a network as claimed. Brown

does not expressly disclose the thermal analysis for final component placement on board layout as cited in the preamble. Such feature is however well known in the art. In fact, Valainis teaches a method and system for analyzing thermal generation in the circuit final placement on design board (see Summary of the Invention). Such thermal analysis provides an effective to place components into the design, change the design physical process, changes of components, component placement changes, etc. (col. 3, lines 9-24, col. 5, lines 1-12, col. 6, lines 42-64).

This would motivate practitioner in the art at the time of the invention was made to combine the teaching in Valainis into the Brown thermal simulator in order to simulate component placement into the integrated circuit design board in a final phase of the design process for placement change, optimize placement design process change, etc. to meet thermal performance of the design.

As per claim 20, Brown and Valainis disclose circuit characteristics being used in the thermal analysis, design characteristics such as thermal characteristics changes for the simulation, etc. as claimed.

As per claim 21, Brown discloses the simulation process is performed over the computer network (pages 5-7).

As per claim 22, Brown discloses documentations for the design process and simulation result of the product design.

As per claim 23, Brown discloses the simulator system allows user to share simulation resources, simulation data, design data, etc. Brown also

discloses output devices being used to plot and print out simulation results [0078]-[0094] as claimed.

As per claim 24, Brown discloses a method and system for analyzing, designing and making integrated circuit product over a computer network with feature limitations very similar to the claimed invention (Field of the Invention and Summary of the Patent). According to Brown, the design method includes:

Identifying circuit component under design to be thermally simulated over the network (page 5, paragraphs [0054], [0055]) for example,

Determining thermal characteristics for a set of circuit components in design [0063] to [0065] for thermal simulation,

Performing thermal simulation for the design ([0055] [0076], [0083], [0087], for example),

Producing result based on thermal design and simulation tool (28) as above, and providing the result to the user over a network as claimed. Brown does not expressly disclose the thermal analysis for final component placement on board layout as cited in the preamble. Such feature is however well known in the art. In fact, Valainis teaches a method and system for analyzing thermal generation in the circuit final placement on design board (see Summary of the Invention). Such thermal analysis provides an effective to place components into the design, change the design physical process, component changes, etc. (col. 3, lines 9-24, col. 5, lines 1-12, col. 6, lines 42-64).

This would motivate practitioner in the art at the time of the invention was made to combine the teaching in Valainis into the Brown thermal simulator in

order to simulate component placement into the integrated circuit design board in a final phase of the design process to make placement change, optimize placement design process, etc. to meet thermal performance of the design.

As per claim 25, Brown and Valainis disclose circuit characteristics being used in the thermal analysis, design characteristics changes for the simulation, etc. as claimed. Brown also discloses the simulation process is performed over the computer network (pages 5-7).

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 5,631,469, issued to Carrieri et al, on May 1997

2. US patent no. 6,578,176 B1, issued to Wang et al, on June 2003

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is 703-305-3812.

3. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 703-308-6647. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

4. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aug. 06, 2004

Thai Phan
Patent Examiner
Art Unit: 2128